APPARATUS FOR MONITORING ASYNCHRONOUS TRANSFER MODE CELLS IN COMMUNICATION SYSTEMS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an asynchronous transfer mode (hereinafter abbreviated ATM) cell monitoring, more particularly, to an asynchronous transfer mode cell monitoring method in communication systems and a system thereof which enable to monitor ATM cells which are being transceived (transmitted/received) between a base transceiver system and a base station controller by specific VPI/VCI, errors of ATM cells, and transmission time of the ATM cells.

2. Background of the Related Art

ATM, which is developed from the packet exchange principle, enables to perform high speed operation as fast as circuit switching does by simplifying a method of processing packets which are being transmitted.

Digital information generated from the ATM is split into blocks each of which has constant length. And, the split blocks to which headers of 5 bytes including receiving numbers respectively are transferred. Other blocks similar to the packets are called cells in ATM.

In a network system, the corresponding cell is transferred to

the opposite party by finding an address of the destination included in the header by cell unit. In a transfer path, the cells arrived from a plurality of terminals are multiplexed in order of arrival sequence and then transferred to the destinations. It is known immediately that the header information of the cell is transferred from a specific terminal, thereby enabling to make a distinction from the multiplex transfer.

As all the cells are transferred after the division, it is not necessary for a physical line to be occupied by one communication. Namely, it is desirable in the efficiency of using a line that ATM cells are transferred through the single line by being multiplexed. It looks like by the transmitting party that a dedicated line is provided for the cells to reach the opposite party by cell transmission through various lines. Such a line is called virtual channel(VC). A number that is called virtual channel identifier(VC) is designated to the virtual channel.

A single virtual channel is established between one terminal and the other terminal, while a plurality of virtual channels are established between sub systems in a telecommunication network. In such intervals, some of the virtual channels are bound together according to the virtual channel identifier each and then a pack of the bound channels is transmitted to the destined terminal. Such a pack of several bound channels together is called a path.

In ATM, the virtual channels are bound by the VCI, whereby the

path is so-called a virtual path having a virtual path identifier(VPI).

Fig. 1 shows a block diagram of an ATM cell monitoring device in an ATM low rate subscriber multiplexing/demultiplexing part of a base station controller according to a related art.

Referring to Fig. 1, a mobile telecommunication system comprises a bas transceiver station 10, a base station controller 20 controlling the base transceiver station, a mobile switching center 30 constituting an interface point for a user traffic between switching centers.

In an ATM cell monitoring device of an ATM low rate subscriber multiplexing/demultiplexing part in a base station controller according to a related art, as shown in Fig. 1, the base transceiver station 10 and the ATM low rate physical layer board assembly(ALPA) 1 are connected each other via 'E1'.

And, an ATM low rate subscriber multiplexing/demultiplexing board assembly 2 functions as an interface between an ATM switch in the base station controller 20 and the base transceiver station 10 for data transceiving, thereby multiplexing and demultiplexing an ATM cell.

Moreover, the ATM low rate subscriber multiplexing/demultiplexing board assembly 2 transmits an ATM cell to an ATM switch in the base station controller 20 and makes an SOC(start of cell) signal of the ATM cell become low active whenever

transmitting a first byte of the ATM cell of 53 bytes, thereby storing the number in a dual port RAM(DPRAM) whenever the SOC signal becomes active. The location written in the dual port RAM is distinguished by indexing with VPI/VCI, which is read by a CPU of the ATM low rate subscriber multiplexing/demultiplexing board assembly 2 to ascertain how many cells 는 passed through by the corresponding VPI/VCI.

In accordance with the number of storage in the dual port RAM, as mentioned in the above explanation, the number of the ATM cells inputted in the base station controller and the other number of the ATM cells outputted from the base station controller are monitored. Unfortunately, the ATM cell monitoring device according to the related art only monitors how many ATM cells are transmitted and received when transceiving an ATM cell consisting of 53 bytes yet fails to monitors an error of the transceiving ATM cell and a delay time of the cell transmission from the base station controller to the base transceiver station.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to an asynchronous transfer mode cell monitoring method in communication systems and a system thereof that substantially obviate one or more of the problems due to limitations and disadvantages of the related art.

The object of the present invention is to provide an

asynchronous transfer mode cell monitoring device in communication systems enabling to monitor an ATM cell error or transmission time when monitoring transceiving ATM cells.

Additional features and advantages of the invention will be set forth in the description which follows and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, the present invention in a communication system including a base transceiver station and a base station controller controlling the base transceiver station includes: a receive interface part established in the base station controller, the receive interface part recording a cell to be monitored in a storage part by checking latched VPI/VCI of asynchronous transfer mode cells received from the base transceiver station by the base station controller, the receive interface part counting the number of error occurrence by checking header errors of the cells; and a transmission interface part established in the base station controller, the transmission interface part transferring a test cell produced for checking a cell transmission time between the base transceiver station and the base station controller to the base transceiver station.

According to the present invention, it is able to monitor an information, a rate of error occurrence and transmission time of the ATM cell transceiving between base transceiver stations.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWING

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiments of the inventing and together with the description serve to explain the principle of the invention.

In the drawings:

Fig. 1 shows a block diagram of an ATM cell monitoring device in an ATM low rate subscriber multiplexing/demultiplexing part of a base station controller according to a related art; and

Fig. 2 shows a block diagram of an asynchronous transfer mode cell monitoring device in a telecommunication system according t the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments

of the present invention, examples of which are illustrated in the accompanying drawings.

Fig. 2 shows a block diagram of an asynchronous transfer mode cell monitoring device in a telecommunication system according t the present invention.

Referring to Fig. 2, an ATM cell monitoring device of a cell multiplexing/demultiplexing device in a base station controller of a communication system includes an E1 matching part 300 consisting of a first to an nth E1 matcher 300a to 300n and enabling to perform E1 interface(2.048Mbps) by being connected to a base transceiver station 100, a multiplexing/demultiplexing part 200(established in a base station controller) multiplexing and transmitting an ATM cell inputted from the E1 matching part 300 to an ATM switch 400 and then demultiplexing the ATM cell inputted from the ATM switch 400, a CPU 270 controlling the multiplexing/demultiplexing part 200, a GPS receiver 280 receiving a packet having a TOD(time of date) information from a GPS 410 and providing the CPU 270 with the packet, an ATM switch 400 switching and outputting ATM cells transceiving with the multiplexing/demultiplexing part 200.

And, the TOD information therein is transferred to the multiplexing/demultiplexing part 200 through the CPU 270.

The multiplexing/demultiplexing part 200 comprises a cell bus 291 through which ATM cells pass, a cell bus RX I/F 210 which multiplexes the ATM cells inputted from the first to nth matcher 300a

to 300n, adjusts the inputted ATM cells for the ATM cell requirements for the multiplexing/demultiplexing part 200 itself, carries out header error check(HEC) of the ATM cells, counts and records the number of error occurred in a first dual port RAM 240, a cell BUS TX I/F 220 transferring an ATM cell received from the ATM switch 400 or a test ATM cell to the E1 matching part 300 wherein the test ATM cell is generated from the CPU 270 for measurement of cell transmission time, a first dual port RAM 240 storing the number of the ATM cells inputted into the multiplexing/demultiplexing part 200 and the other number of the error-occurred ATM cells of the inputted ATM cells which are provided by the cell bus RX/I/F 210, a second dual port RAM 250 in which VPI index matched by each of the VPI/VCI is stored, a CAM(content addressable memory) 260 in which an address of the second dual port RAM 250 where the VPI index is stored, a first FIFO(first in first out) 280 storing temporarily the ATM cells received from the E1 matching part 300 wherein the ATM cells are to be read by the CPU 270, and a second FIFO(290) storing temporarily the test ATM cells generated from the CPU 270.

The ATM cell monitoring device in a communication system of the above-described structure according to the present invention may be mainly divided into three parts.

First, the CPU 270 monitors information of the cell to be monitored by comparing VPI/VCI of the ATM cells inputted to the multiplexing/demultiplexing part 200 to the other VPI/VCI latched

by hardware.

Second, the cell bus RX I/F 210 counts the number of the error-occurring ATM cells by carrying out header error checks of the ATM cells inputted to the cell bus RX/ I/F 210 itself.

Third, how long the cell transferring time takes for transceiving loop is found out by transceiving the test ATM cells between the multiplexing/demultiplexing part 200 being the ATM low rate subscriber multiplexing/demultiplexing board assembly(ALMA) and the base transceiver station 100.

First of all, it is established to monitor the ATM cells consisting of 53 bytes each so that the value of 24 bits of the VPI/VCI field is latched with hardware wherein VPI and VCI is of 8 bits and 16 bits respectively at the user network interface.

When the ATM cells to be monitored selectively exists by comparing the VPI/VCI of the ATM cells inputted to the cell bus RX/ I/F 270 to the other VPI/VCI latched with hardware, the CPU 270 directs the first FIFO 230 to store it when the cell bus RX/ I/F 210 receives the ATM cells having the VPI/VCI field. In accordance with the direction, once the ATM cell to be monitored out of the whole ATM cells received by the base transceiver station 100 is received by the cell BUS RX I/F 210 and then recorded in the first FIFO 230, the CPU 270 checks the error occurrence through the entire cells by monitoring the recorded ATM cell of 53 bytes.

Then, the header error check of the ATM cell inputted from a

cell bus 291 is carried out by the cell bus RX I/F 210. And, the cell bus RX I/F 210 transmits the cell transferred from the base transceiver station 100 to the ATM switch 400 as soon as stores the number of the error-occurring ATM cells and the other number of the ATM cells inputted to the multiplexing/demultiplexing part 200 in the first dual port RAM 240. Said cell bus RX I/F 210 is realized by a field programmable logic gate array(FPGA).

In this case, when the VPI/VCI of the ATM cell inputted to the multiplexing/demultiplexing part 200 is matched with a reference value of the CAM 260, said CAM 260 outputs a data to be used as an address of the second dual port RAM 250. And, said VPI/VCI has a value latched with hardware.

Storing the VPI index values by each VPI/VCI, the second dual port RAM 250 outputs a VPI index corresponding to the latched VPI/VCI. The VPI index values by each VPI/VCI which are outputted from the second dual port RAM 250 are used for addresses in the first dual port RAM 240, thereby determining where the number of the error-occurring ATM cells and the other number of the ATM cells inputted into the multiplexing/demultiplexing part 200 will be recoded therein.

In this case, the data of the CAM 260 and the second dual port RAM 250 are recorded when electric power is inputted to the CPU 270 with software and may be adjusted occasionally on operation.

Loop time of the ATM cell transceiving between the base station

controller and the base transceiver station 100 is checked in a manner as follows.

The CPU 270 generates a test cell in the second FIFO 290. And, when the generated test cell is transmitted to the base transceiver station 100 and then loop-backed to the cell bus RX I/F 210 of the base station controller, the GPS receiver 280 puts the TOD information at the time when transferred from the cell bus TX I/F 220 to the base transceiver station 100 and the time information at the time that the cell is received by the cell bus RX I/F 210 from the base transceiver station 100 in the test ATM cell. In this case, the time information is transmitted from the GPS 410.

Therefore, once the cell loop-backed from the base transceiver station 100 arrives in the cell multiplexing/demultiplexing part device and is stored in the first FIFO 230 by being received from the cell bus RX I/F 210, the CPU 270 enables to monitor the loop time(cell transmission delay time) by each VPI/VCI by comparing the transmission and receive time each other.

Namely, the VPI/VCI of the test cell is recognized as a cell to be monitored by the cell bus RX I/F and then stored in the first FIFO 230, whereby the CPU 270 checks the transceiving time of the test cell.

As mentioned in the above explanation, the apparatus for monitoring asynchronous transfer mode cells in communication systems according to the present invention has the effects as follows.

First, it is able to monitor the required contents of the ATM cell of 53 bytes being transceived between the base transceiver station and the base station controller.

Second, it is able to monitor an error rate of the ATM cells being transceived the base transceiver station and the base station controller.

Third, it is able to monitor the transmission(delay) time of the ATM cells the base transceiver station and the base station controller.

It will be apparent to those skilled in the art that various modifications and variations can be made in an apparatus for monitoring asynchronous transfer mode cells in communication systems of the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and equivalents.